providing a ~~second~~ plurality of memory banks of semiconductor memory devices, each memory bank being accessible to the ~~first and~~ second processors for operations selected from the group comprising read and write operations; and

storing subsets of said audio data in the second plurality of memory banks, the subsets corresponding to different groups of audio channels.

3. (Amended) The ~~method~~ of claim 1 wherein [P is equal to two] the second plurality of memory banks includes two memory banks.

5. (Twice Amended) A system having first and second buses for processing real-time audio data from a first plurality of audio channels, the system comprising:

a first processor and a second processor coupled to said first and second busses, respectively; and

a second plurality of memory banks of semiconductor memory devices coupled to said first and second buses for storing said audio data, said second plurality of memory banks being accessible to the first and second processors for operations selected from the group comprising read and write operations, said second plurality of memory banks storing subsets of audio data, said subsets corresponding to different groups of audio channels.

6. ~~(Amended)~~ The system of claim 5 further comprises [P] a plurality of selectors coupled said first and second buses to select said memory banks ~~for access~~ by one of said first and second processors.

7. (Amended) The ~~system of claim 6~~ wherein [P] the plurality of selectors include [P] a plurality of address multiplexers and [P] data transceivers.

10. (Amended) The system of claims 5, wherein the [P] memory banks include dynamic random access memories.